REMARKS

This Amendment is in response to the Office Action dated September 25, 2001. Claims 1-16 are pending in the present application. Applicant has amended claim 1. Consequently, claims 1-16 remain pending in the present application.

Applicant has amended claim 1 to correct a minor error, replacing "lease" with "least." Applicant respectfully submits that this amendment does not narrow the scope of claim 1. Applicant has also amended claim 1 to recite that the silicide does not reside between the gates of the gate stack. Support for this amendment can be found in the specification, page 12, lines 5-12 and Figures 3B and 5B. Applicant respectfully submits that no new matter is added.

In the above-mentioned Office Action, the Examiner rejected claims 1-7 under 35 U.S.C. § 103 as being unpatentable over Applicant's admitted prior art ("AAPA") in view of by U.S. Patent No. 5,065,220 ("Paterson").

Applicant respectfully disagrees with the Examiner's rejection. Claim 1 recites:

> [a] flash memory device comprising:
> a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;
> at least one component including a polysilicon layer having a top surface;
> a silicide on the top surface of the polysilicon layer of the at least one component;
> an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein, the plurality of contact holes being formed by etching the insulating layer to provide the plurality of contact holes, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer; and
> a conductor for filling the plurality of contact holes;
> wherein the silicide layer resides on the first polysilicon layer but not between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks.

Thus, although the silicide layer covers the polysilicon layer of the at least one

component, the silicide layer does not cover the layers within the plurality of gate stacks such that the silicide layer is not beween the gates of the gate stack. The flash memory device of claim 1 includes a silicide layer on the first polysilicon layer, but not between the gates of the gate stacks. The silicide layer allows for better electrical contact to the component. Specification, page 13, lines 4-6. Moreover, the silicide layer acts as an etch stop to prevent over-etching of the polysilicon component and destruction of field insulating regions during etching of contact holes. Specification, page 13, lines 1-4.

As the Examiner has acknowledged, the AAPA does not "teach a silicide on the top surface of the polysilicon layer of the at least one component, and the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer." Instead, the AAPA merely discloses the presence of gate stacks and polysilicon components, with contact holes that have been etched in the insulating layer. Specification, page 2, line 22-page 3, line 20 and Figures 2A and 2B.

Paterson describes a semiconductor device including capacitors. Paterson, Abstract, lines 1-3. In order to form the capacitor, a polysilicon layer with a silicide layer is used as the lower plate of the capacitor. Paterson, col. 2, lines 42-45. The silicide layer is provided "for additional stability of the capacitor 2." Paterson, col. 2, lines 49-50. The silicide layer thus resides between the bottom and top plates of the capacitor. Paterson, col. 2, lines 42-58 and Fig. 1. During formation, a first polysilicon layer is formed, and the silicide formed on that first polysilicon layer for all of the devices, including but not limited to the capacitor. Paterson, col. 3, lines 13-61. The silicide is used to enhance the voltage stability of the capacitor, though other structures are all silicided at the same, first polysilicon layer. Paterson, col. 3, lines 54-61 and Figs. 2a-2h

(silicide film 14).

One of ordinary skill in the art would not be motivated to combine the AAPA with Paterson in the manner suggested by the Examiner. As discussed above, Paterson is concerned with the formation of capacitors in a device. Paterson utilizes the silicide film in order to stabilize the capacitor. The AAPA, in contrast, is concerned with the formation of gate stacks and devices, such as devices formed using the first polysilicon layer. The AAPA fails to discuss the use of capacitors in conjunction with the gate stacks. As a result, one of ordinary skill in the art would not be motivated to combine the teachings of Paterson, which relate to capacitors, with those of the AAPA, which relate to gate stacks and polysilicon layer devices. More specifically, one of ordinary skill in the art would not be motivated to provide the silicide layer used to stabilize a capacitor and described in the teachings of Paterson in the device described in the AAPA. Consequently, the AAPA in view of Paterson cannot teach or suggest the flash memory device recited in claim 1.

Even if Paterson were added to the teachings of the AAPA, the combination would fail to teach or suggest the recited flash memory device. Paterson teaches that the silicide layer is provided on first (lowest) polysilicon all of the devices. Consequently, if the silicide layer of Paterson was used in the AAPA, a first polysilicon layer would be deposited and silicided. Other layers would be provided on this silicided polysilicon layer to form devices. Thus, this silicided polysilicon layer would typically be present in the gate stacks, for example as the floating gate, and other devices. Consequently, a portion of the silicide layer would reside between the floating gate and the control gate in each gate stack. This is contrary to the silicide layer recited in claim 1 and described in the specification. As a result, even if the teachings of Paterson are added to

those of the AAPA, the combination would still fail to teach or suggest that the silicide layer on the first component that resides on the first polysilicon layer does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks. The AAPA in view of Paterson, therefore, cannot teach or suggest the flash memory device recited in claim 1. Accordingly, Applicant respectfully submits that claim 1 is allowable over the cited references.

Claims 2-6 depend on independent claim 1. Consequently, the arguments herein apply with full force to claims 2-6. Thus, Applicant respectfully submits that claims 2-6 are allowable over the cited references.

In view of the foregoing, it is submitted that the claims in the application are patentable over the cited reference and are in condition for allowance. Reconsideration of the rejections and objections is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;

at leas[e]t one component including a polysilicon layer having a top surface;

a silicide on the top surface of the polysilicon layer of the at least one component;

an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein, the plurality of contact holes being formed by etching the insulating layer to provide the plurality of contact holes, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer; and

a conductor for filling the plurality of contact holes;

wherein the silicide layer resides on the first polysilicon layer but not between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks.